Remarks

The Final Office Action dated September 22, 2009 listed the following new grounds of rejection: claims 6-7, 10-14, 17 and 20-24 stand rejected under U.S.C. § 103(a) over Rhee (U.S. Patent No. 6,667,525) in view of Suguro (U.S. Patent Pub. 2001/0039107 and further in view of Tao (U.S. Patent No. 6,399,515); and claims 8 and 18-19 stand rejected under U.S.C. § 103(a) over the '525, '107 and '515 references in view of Lee (U.S. Patent No. 6,172,399). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 103(a) rejections of claims 6-14 and 17-24 because the Examiner fails to provide a valid reason for the proposed combination of the asserted references, thus also failing to cite evidence of motivation for modifying the '525 reference. Consistent with M.P.E.P. § 2143.01 and relevant case law, a § 103 rejection must provide evidence of motivation where a proposed combination of references would modify a primary reference. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner asserts that the skilled artisan would combine the grain sizes of metal gate electrode 3 of the '107 reference with the semiconductor gate layers 23 and 24 of the '525 reference "to reduce the variations in threshold voltage." However, this hypothetical combination lacks any supporting evidence, and further does not provide a clearly-articulated reason (or explanation as to how the '525 reference could or would operate as modified), that would be consistent with the *KSR* decision.

Unlike the *KSR* decision, where the combination involved combining "two known devices according to their established functions", the Examiner's proposed combination does not involve simply combining teachings in which the cited references are not modified in their operation. More specifically, the '525 and '107 references are directed to different types of devices that use different types of gate materials. The '525 reference teaches using a lower poly-SiGe layer 23 and an upper poly-Si layer 24 (*see, e.g.,* Figure 3 and Col, 5:5-23), whereas the '107 reference teaches that its gate electrode is made of a

metal or metallic compound with the gate being formed of a single type of material (*see, e.g.,* paragraphs 0028, 0082 and 0084). As such, the Examiner's combination would necessarily involve (extensively) modifying the cited teachings of the '525 and '107 references. The '107 reference also does not teach that using its grain sizes (specified for a metal gate electrode) in the doped semiconductor materials of the '525 reference would "reduce the variations in threshold voltage" as asserted by the Examiner. Accordingly, the Examiner's unsupported and unexplained assertion that "it would have been obvious" in support of the modification is insufficient. *KSR* and M.P.E.P. § 2141 make it clear that such assertions are inapplicable where the operation of one of the references is modified.

Moreover, according to M.P.E.P. § 2141, Applicant can rebut such assertions of obviousness simply by showing that "the elements in combination do not merely perform the function that each element performs separately." This is also consistent with various parts of the *KSR* decision, which repeatedly refer to combined teachings in which the cited references are not modified in their operation. In view of the above, the elements are not merely the same as before combination. As such, in the context of the *KSR* decision, the asserted combination "as a whole" is entirely unpredictable based on the asserted teachings of the '525 and '107 references.

Moreover, in view of the Examiner's failure to cite any supporting evidence or articulate a valid reason for the proposed combination, Applicant submits that the proposed combination appears to be improperly based on Applicant's disclosure in a hindsight reconstruction of the claimed invention. *See, e.g.,* M.P.E.P. § 2142.

In addition, the Examiner fails to address aspects of the claimed invention directed to the first layer of gate material being activated crystalline material. The '525 reference does not teach that lower poly-SiGe layer 23 (*i.e.,* the asserted first layer of gate material) is activated crystalline material. Applicant submits that the '107 reference also does not teach such aspects, but instead teaches using metal as the gate material (as discussed above).

In view of the above, the § 103(a) rejections of claims 6-14 and 17-24 are improper and Applicant requests that they be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 8, 18 and 19 because the Examiner has failed to answer Applicant's traversals as required under M.P.E.P.

§ 707.07(f). Specifically, the Examiner improperly continues to assert that the '399 reference corresponds to aspects of these claims without responding to Applicant's previous arguments regarding the impropriety of the previously-asserted correspondence as required. In at least two responses of record, Applicant has explained in detail that the cited portions of the '399 reference are unrelated to aspects of claims 8, 18 and 19 directed to a doping implant in the activated gate material having a certain abruptness of a doping profile. In violation of M.P.E.P. § 707.07(f), the Examiner continues to assert correspondence to claims 8, 18 and 19 based on the same portion of the '399 reference (*i.e.,* Col. 1:54-58) without responding in any manner to Applicant's previous arguments.

In view of the above, the (uncontroverted) record establishes that the § 103 rejection fails. As previously discussed, the cited portions of the '399 reference discuss the abruptness of the junction dopant profile in a source/drain implant shallow junction (*see, e.g.,* Col. 1:41-58), instead of teaching that the abruptness of the doping profile in activated gate material is above a certain level, as in the claimed invention. Moreover, the '399 reference does not teach or suggest that modifying layer 23 of the '525 reference to have an abruptness of a doping profile of about 10 nm or less would result in "better threshold voltage roll-off characteristics"; instead the cited portions of the '399 reference teach that a source/drain junction profile abruptness of less than 10 nm addresses poor threshold voltage roll-off characteristics. Applicant submits that the cited portions of the '399 reference concerning source/drain junctions are unrelated to the claimed invention, which includes aspects directed to the abruptness of the doping profile in a gate electrode. Accordingly, the § 103(a) rejection of claims 8, 18 and 19 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claim 9 because the modification of the '525 reference proposed by the Examiner would render the '525 reference unsatisfactory for its intended purpose. Consistent with the above-cited *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('525) reference - the rationale being that the prior art teaches away from such a modification. *See KSR* at 1742 ("[W]hen the prior art teaches away

from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.").

In this instance, the Examiner proposes to modify the '525 reference such that upper layer 24 of the gate is formed of amorphous silicon. The intended purpose of the '525 reference, however, is to restrain the diffusion of Ge through the grain boundary from the lower layer 23 to the upper layer 24 by giving the lower layer 23 a columnar crystalline structure and the upper layer 24 random crystalline structure. *See, e.g.,* Col. 4:50 to Col. 5:22 and Figure 3. Applicant submits that replacing the '525 reference's random crystalline structure upper layer 24 with a layer of amorphous silicon would render the '525 reference unsatisfactory for restraining the diffusion of Ge through the grain boundary. As such, the '525 reference teaches away from such a modification and there is no motivation for the skilled artisan to modify the '525 reference in the manner proposed by the Examiner. Applicant notes that the Examiner has previously proposed the same modification of the '525 reference (*see, e.g.,* page 4 of the Office Action dated August 8, 2008). Thus, the Examiner has also improperly reintroduced the rejection of claim 9 without responding to Applicant's previous arguments regarding the impropriety of the proposed modification in violation of M.P.E.P. § 707.07(f). Accordingly, the § 103(a) rejection of claim 9 is improper for lack of motivation and further for the Examiner's failure to address Applicant's traversals and Applicant requests that it be withdrawn.

Moreover, the Examiner fails to cite to any reference that teaches a layer of amorphous gate material that has a grain size that is at least twice as large as the grain size of a layer of activated crystalline gate material. As acknowledged by the Examiner, the '525 reference does not teach that the second layer of gate material consists of amorphous gate material. The '300 reference, however, fails to disclose any grain size for the cited second gate conductor 20, let alone teach that the second gate conductor 20 has a grain size that is at least twice as large as the grain size of the first gate conductor layer 14. Because neither reference teaches these aspects, no reasonable combination of these references can provide correspondence to the claimed invention. As such, the § 103 rejection of claim 9 fails.

Applicant further traverses the § 103(a) rejection of claim 20 because the Examiner fails to establish a *prima facie* case of obviousness with regard to the claimed grain size of Applicant's second layer of gate material. According to M.P.E.P. § 2144.05, the Examiner must first establish that the claimed ranges "overlap or lie inside ranges disclosed by the prior art" to establish a *prima facie* case of obviousness. In this instance, the '107 reference does not teach that the grain size in the second layer is below about 30 nm, as claimed. Instead, the '107 reference teaches that the metal gate electrode 3' (*i.e.,* the asserted second layer) has a grain size of more than 30 nm (*see, e.g.,* paragraph 0094). Thus, the Examiner has failed to establish a *prima facie* case of obviousness since the '107 reference does not disclose a range that overlaps the claimed range. Accordingly, the § 103(a) rejection of claim 20 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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